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What is claimed is:

1. Semiconductor structure, comprising:

a buried first semiconductor layer of a first doping type;

a second semiconductor layer of the first doping type on the buried semiconductor layer, which is less doped than the buried first semiconductor layer;

a semiconductor area of a second doping type on the second semiconductor layer, so that a pn junction is formed between the semiconductor area and the second semiconductor layer; and

a recess present below the semiconductor area in the buried first semiconductor layer, which contains a semiconductor material of the first doping type, which lies deeper in the substrate than the buried first semiconductor layer, such that the breakdown voltage across the pn junction is higher than if the recess were not provided.

2. Semiconductor structure according to claim 1, wherein the second semiconductor layer extends into the recess and the recess further has another semiconductor area of the first doping type, which is heavier doped than the second semiconductor layer.

3. Semiconductor structure according to claim 2, wherein the further semiconductor area is doped equal or less than the buried first semiconductor layer.

4. Semiconductor structure according to claim 1, wherein the recess fully penetrates the buried first semiconductor layer.

5. Semiconductor structure according to claim 1, wherein the semiconductor area is a base, the first buried

semiconductor layer a subcollector and the second semiconductor layer a collector of a bipolar transistor.

6. Semiconductor structure according to claim 5, wherein the buried first semiconductor layer further represents a subcollector for at least another bipolar transistor, wherein the buried first semiconductor layer has no or such recess for at least another bipolar transistor, that the bipolar transistors have different breakdown voltages.

7. Semiconductor structure according to claim 6, wherein the buried first semiconductor layer has recesses of different widths for the bipolar transistors.

8. Method for providing a semiconductor structure according claim 1, further comprising:

providing the buried first semiconductor layer with the recess formed therein;

generating the further semiconductor area in the recess;

introducing the semiconductor material of the first doping type into the recess, wherein after the step of introducing the semiconductor material lies deeper in the substrate than the buried first semiconductor layer;

generating the second semiconductor layer on the buried first semiconductor layer, which is less doped than the buried first semiconductor layer;

generating the semiconductor area on the second semiconductor layer.

9. Method according to claim 8, wherein the step of providing comprises:

depositing an implantation mask on a semiconductor substrate, wherein the implantation mask covers the recess;

implanting the buried first semiconductor layer by using the implantation mask.

10. Method according to claim 8, further comprising:

depositioning a further implantation mask, which leaves a recess exposed, after the step of providing;

generating a further semiconductor area in the recess by using the further implantation mask.

11. Method according to claim 8, further comprising:

depositing a further implantation mask, which leaves the recess exposed, after the step of generating the second semiconductor layer and

generating a further semiconductor area in the recess by using the further implantation mask.